Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	mosfet with simultaneously with (slit adj1 gate).bi.	US-PGPUB; USPAT	OR	ON	2005/08/18 13:49
S2	0	(mosfet transistor cmos) with (polysilicon electrode) with (slit adj1 gate).bi.	US-PGPUB; USPAT	OR	ON	2005/08/18 14:08
S3	489	mosfet with simultaneously with (gate).bi.	US-PGPUB; USPAT	OR	ON	2005/08/18 13:50
S4	194	S3 and (high$3 adj1 voltage)	US-PGPUB; USPAT	OR	ON	2005/08/18 13:51
S5	33	(wu-haw-chuan tzeng-jiann-tyng ho-david).in.	US-PGPUB; USPAT	OR	ON	2005/08/18 14:07
S6	0	((flash adj1 memory) with MOSFET) same ((dielectric insulat$3) with simultaneously with substrate).bi.	US-PGPUB; USPAT	OR	ON	2005/08/18 14:14
S7	1	((flash adj1 memory) with MOSFET) and ((dielectric insulat$3) with simultaneously with substrate).bi.	US-PGPUB; USPAT	OR	ON	2005/08/18 14:15
S8	167	(((flash adj1 memory) (split adj1 gate)) with MOSFET) and simultaneously.bi.	US-PGPUB; USPAT	OR	ON	2005/08/18 14:50
S9	5	(high adj voltage adj MOSFET) with ((memory adj1 cell) (flash adj1 memory)).bi.	US-PGPUB; USPAT	OR	ON	2005/08/18 14:56
S10	4	((memory adj1 cell) with (logic adj1 cell)) and ((dielectric insulat$3) with simultaneously).bi.	US-PGPUB; USPAT	OR	ON	2005/08/18 15:07
S11	0	(EPROM with MOSFET) same ((dielectric insulat$3) with simultaneously).bi.	US-PGPUB; USPAT	OR	ON	2005/08/18 15:12
S12	130	(EPROM with MOSFET).bi.	US-PGPUB; USPAT	OR	ON	2005/08/18 15:12
S13	124	S12 not (S4 S5 S8 S9)	US-PGPUB; USPAT	OR	ON	2005/08/18 15:13